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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))</small>	Attorney Docket No.	P3814
	First Inventor or Application Identifier	Mario Nemirovsky et al.
	Title	Methods and Apparatus for Background Memory Management
	Express Mail Label No.	EJ745193044US

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>	ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231
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<p>1. <input checked="" type="checkbox"/> * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)</p> <p>2. <input checked="" type="checkbox"/> Specification [Total Pages 18] (preferred arrangement set forth below)</p> <ul style="list-style-type: none">- Descriptive title of the invention- Cross References to Related Applications- Statement Regarding Fed sponsored R & D- Reference to Microfiche Appendix- Background of the invention- Brief Summary of the invention- Brief Description of the Drawings (if filed)- Detailed Description- Claim(s)- Abstract of the Disclosure <p>3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 3]</p> <p>4. Oath or Declaration [Total Pages 2]</p> <p>a. <input checked="" type="checkbox"/> Newly executed (original or copy)</p> <p>b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed)</p> <p>i. <input type="checkbox"/> <u>DELETION OF INVENTOR(S)</u> Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).</p>	<p>5. <input type="checkbox"/> Microfiche Computer Program (Appendix)</p> <p>6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)</p> <p>a. <input type="checkbox"/> Computer Readable Copy</p> <p>b. <input type="checkbox"/> Paper Copy (identical to computer copy)</p> <p>c. <input type="checkbox"/> Statement verifying identity of above copies</p>
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ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))

8. ☐ 37 C.F.R. § 3.73(b) Statement ☒ Power of Attorney
(when there is an assignee)

9. ☐ English Translation Document (if applicable)

10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations

11. ☐ Preliminary Amendment

12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

13. ☒ * Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
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14. ☐ Certified Copy of Priority Document(s)
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Docket Number (Optional)
P3814

Applicant or Patentee: Mario Nemirovsky, et al.
Application or Patent No.: NA
Filed or Issued: NA
Title: Methods and Apparatus for Background Memory Management

I hereby declare that I am

- ☐ the owner of the small business concern identified below:
☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF SMALL BUSINESS CONCERN XStream Logic, Inc.

ADDRESS OF SMALL BUSINESS CONCERN 750 University Ave., Suite 270, Los Gatos, CA 95032-7698

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time, or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in:

- ☒ the specification filed herewith with title as listed above.
☐ the application identified above.
☐ the patent identified above.

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- Each person, concern, or organization having any rights in the invention is listed below:
☒ no such person, concern, or organization exists.
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NAME OF PERSON SIGNING Mario Nemirovsky

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SIGNATURE _____ DATE _____

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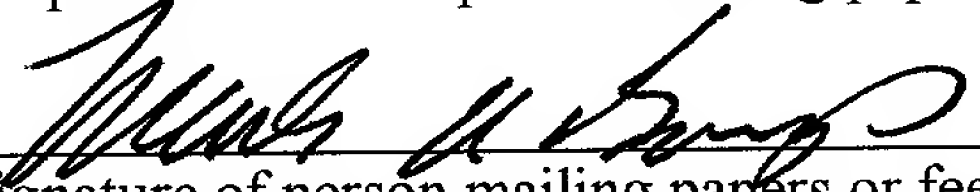
Title of Case: Methods and Apparatus for Background Memory Management

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1. Utility patent application transmittal.
2. 18 sheets of specification.
3. 3 sheets of drawings.
4. Fee transmittal.
5. Duplicate fee transmittal.
6. Declaration and Power of Attorney.
7. Verified Statement Claiming Small Entity.
8. Check for fees in the amount of \$420.00.
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Mark A. Boys

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Methods and Apparatus for Background Memory Management

*by inventors Mario Nemirovsky, Naren Sankar,
Adolfo Nemirovsky and Enric Musoll*

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Field of the Invention

The present invention is in the area of integrated circuit
10 microprocessors, and pertains in particular to memory management, and the
use of microprocessor resources in such management.

Background of the Invention

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Microprocessors, as is well-known in the art, are integrated circuit
(IC) devices that are enabled to execute code sequences which may be
generalized as software. In the execution most microprocessors are capable
of both logic and arithmetic operations, and typically modern
20 microprocessors have on-chip resources (functional units) for such
processing.

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Microprocessors in their execution of software strings typically
operate on data that is stored in memory. This data needs to be brought into
the memory before the processing is done, and sometimes needs to be sent
out to a device that needs it after its processing.

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There are in the state-of-the-art two well-known mechanisms to
bring data into the memory and send it out to a device when necessary. One
mechanism is loading and storing the data through a sequence of
Input/Output (I/O) instructions. The other is through a direct-memory
access device (DMA).

In the case of a sequence of *I/O* instructions, the processor spends significant resources in explicitly moving data in and out of the memory. In the case of a DMA system, the processor programs an external hardware circuitry to perform the data transferring. The DMA circuitry performs all of the required memory accesses to perform the data transfer to and from the memory, and sends an acknowledgement to the processor when the transfer is completed.

In both cases of memory management in the art the processor has to explicitly perform the management of the memory, that is, to decide whether the desired data structure fits into the available memory space or does not, and where in the memory to store the data. To make such decisions the processor needs to keep track of the regions of memory wherein useful data is stored, and regions that are free (available for data storage). Once that data is processed, and sent out to another device or location, the region of memory formerly associated with the data is free to be used again by new data to be brought into memory. If a data structure fits into the available memory, the processor needs to decide where the data structure will be stored. Also, depending on the requirements of the processing, the data structure can be stored either consecutively, in which case the data structure must occupy one of the empty regions of memory; or non-consecutively, wherein the data structure may be partitioned into pieces, and the pieces are then stored into two or more empty regions of memory.

An advantage of consecutively storing a data structure into memory is that the accessing of this data becomes easier, since only a pointer to the beginning of the data is needed to access all the data.

When data is not consecutively stored into the memory, access to the data becomes more difficult because the processor needs to determine the explicit locations of the specific bytes it needs. This can be done either in

software (i.e. the processor will spend its resources to do this task) or in hardware (using a special circuitry). A drawback of consecutively storing the data into memory is that memory fragmentation occurs. Memory fragmentation happens when the available chunks of memory are smaller than the data structure that needs to be stored, but the addition of the space of the available chunks is larger than the space needed by the data structure. Thus, even though enough space exists in the memory to store the data structure, it cannot be consecutively stored. This drawback does not exist if the data structure is allowed to be non-consecutively stored.

Still, a smart mechanism is needed to generate the lowest number of small regions, since the larger the number of small regions that are used by a data structure, the more complex the access to the data becomes (more specific regions need to be tracked) regardless of whether the access is managed in software or hardware as explained above.

What is clearly needed is system for background management of memory in systems where large amounts of data must be moved to and from a memory for processing.

Summary of the Invention

In a preferred embodiment of the present invention a background memory manager (BMM) for managing a memory in a data processing system is provided, the BMM comprising circuitry for transferring data to and from an outside device and to and from a memory, a memory state map associated with the memory, and a communication link to a processor. The BMM manages the memory, performing all data transfers between the

outside device and the memory, and maintains the memory state map according to memory transactions made.

5 In preferred embodiments the BMM, after storing a data structure into the memory, provides a data identifier for the structure on the link to the processor. Also in preferred embodiments, the BMM, in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

10 In some embodiments the BMM, in response to a signal on the processor link that the processor is finished with certain identified data in the memory, copies the data from the memory to another device, and updates the memory state map to indicate the region of the data copied. There may further be an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory. The BMM in
15 preferred embodiments is particularly suited for handling data packets in a packet processing router.

In another aspect of the invention a data processing system is provided, comprising a processor, a memory coupled to the processor, and a background memory manager coupled to the memory and the processor, the
20 background memory manager including circuitry for transferring data to and from an outside device and to and from the memory, and a memory state map associated with the memory. The BMM manages the memory, performing all data transfers between the outside device and the memory, and maintains the memory state map according to memory transactions
25 made.

In preferred embodiments of the system the BMM, after storing a data structure into the memory, provides a data identifier for the structure to the processor. Also in preferred embodiments the BMM, in making memory

transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

5 In some embodiments of the system the BMM, in response to a signal from the processor that the processor is finished with certain identified data in the memory, copies the data from the memory to another device, and updates the memory state map to indicate the region of the data copied. In some embodiments there is an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the
10 memory. The data processing system is particularly suited to processing data packets in Internet packet processors.

In yet another aspect of the invention a network packet router is provided, comprising an input/output (I/O) device for receiving and sending packets on the network, a processor, a memory coupled to the processor,
15 and a background memory manager coupled to the memory and the processor, the background memory manager including circuitry for transferring packets to and from the I/O device and to and from the memory, and a memory state map associated with the memory. The BMM manages the memory, performing all packet transfers between the I/O device and the
20 memory, and maintains the memory state map according to memory transactions made.

In a preferred embodiment the BMM, after storing a packet into the memory, provides a data identifier for the packet to the processor. Also in a preferred embodiment the BMM, in making memory transactions, updates
25 the memory state map to the new memory state, keeping track of regions occupied by valid packets and regions not occupied by valid packets.

In some embodiments the BMM, in response to a signal that the processor is finished with a packet in the memory, copies the packet from

the memory to the I/O device, and updates the memory state map to indicate the region of the packet copied. There may also be an interrupt handler allowing the I/O device to interrupt the BMM when packets are available to be transferred to the memory.

5 In still another aspect of the present invention a method for managing a memory in a data processing system is provided, comprising the steps of (a) transferring data to and from an outside device and to and from the memory by circuitry in a background memory manager (BMM); (b) updating a memory state map associated with the memory in the BMM each time a
10 memory transaction is made; and (c) notifying a processor with memory state data each time a change is made.

In preferred embodiments of the method, in step (c), the BMM, after storing a data structure into the memory, provides a data identifier for the structure on the link to the processor. Also in preferred embodiments the
15 BMM, in step (b), in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

In some embodiments, in step (a), the BMM, in response to a signal that the processor is finished with certain identified data in the memory,
20 copies the data from the memory to another device, and updates the memory state map to indicate the region of the data copied. There may further be a step for interrupting the BMM by the outside device when data is available to be transferred to the memory. The method is particularly well suited for processing data packets in a packet router, such as in the Internet.

25 In embodiments of the invention, taught in enabling detail below, for the first time an apparatus and methods are provided for complete background memory management, freeing processor power in systems like

Internet packet routers, to accomplish more processing, by not being required to do memory management.

5

Brief Description of the Drawing Figures

Fig. 1 is a simplified diagram of memory management by direct I/O processing in the prior art.

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Fig. 2 is a simplified diagram of memory management by direct memory access in the prior art.

Fig. 3 is a diagram of memory management by a Background Memory Manager in a preferred embodiment of the present invention.

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Description of the Preferred Embodiments

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Fig. 1 is a simplified diagram of memory management in a system 104 comprising a processor 100 and a memory 102 in communication with a device 106. In this example it is necessary to bring data from device 106 into memory 102 for processing, and sometimes to transmit processed data from memory 102 to device 106, if necessary. Management in this prior art example is by processor 100, which sends I/O commands to and receives responses and/or interrupts from device 106 via path 108 to manage movement of data between device 106 and memory 102 by path 110. The processor has to determine whether a data structure can fit into available space in memory, and has to decide where in the memory to store incoming data structures. Processor 100 has to fully map and track memory blocks

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into and out of memory 102, and retrieves data for processing and stores results, when necessary, back to memory 102 via path 114. This memory management by I/O commands is very slow and cumbersome and uses processor resources quite liberally.

5 Fig. 2 is a simplified diagram of a processor system 200 in the prior art comprising a processor 100, a memory 102 and a direct memory access (DMA) device 202. This is the second of two systems by which data, in the conventional art, is brought into a system, processed, and sent out again, the first of which is by I/O operations as described just above. System 200
10 comprises a DMA device 202 which has built-in intelligence, which may be programmed by processor 100, for managing data transfers to and from memory 102. DMA device 202 is capable of compatible communication with external device 106, and of moving blocks of data between device 102 and 106, bi-directionally. The actual data transfers are handled by DMA
15 device 202 transparently to processor 100, but processor 100 must still perform the memory mapping tasks, to know which regions of memory are occupied with data that must not be corrupted, and which regions are free to be occupied (overwritten) by new data.

In the system of Fig. 2 DMA processor 100 programs DMA device
20 202. This control communication takes place over path 204. DMA device 202 retrieves and transmits data to and from device 106 by path 208, and handles data transfers between memory 102 and processor 100 over paths 204 and 206.

In these descriptions of prior art the skilled artisan will recognize that
25 paths 204, 206 and 208 are virtual representations, and that actual data transmission may be by various physical means known in the art, such as by parallel and serial bus structures operated by bus managers and the like, the bus structures interconnecting the elements and devices shown.

Fig. 3 is a schematic diagram of a system 300 including a Background Memory Manager (BMM) 302 according to an embodiment of the present invention. BMM 302 a hardware mechanism enabled to manage the memory in the background, i.e. with no intervention of the processor to
5 decide where the data structure will be stored in the memory. Thus, the processor can utilize its resources for tasks other than to manage the memory.

The present invention in several embodiments is applicable in a general way to many computing process and apparatus. For example, in a
10 preferred embodiment the invention is applicable and advantageous in the processing of data packets at network nodes, such as in routers in packet routers in the Internet. The packet processing example is used below as a specific example of practice of the present invention to specifically describe apparatus, connectivity and functionality.

15 In the embodiment of a packet router, device 106 represents input/output apparatus and temporary storage of packets received from and transmitted on a network over path 308. The network in one preferred embodiment is the well-known Internet network. Packets received from the Internet in this example are retrieved from device 106 by BMM 302, which
20 also determines whether packets can fit into available regions in memory and exactly where to store each packet, and stores the packets in memory 102, where they are available to processor 100 for processing. Processor 100 places results of processing back in memory 102, where the processed packets are retrieved, if necessary, by BMM on path 312 and sent back out
25 through device 106.

In the embodiment of Fig. 3 BMM 302 comprises a DMA 202 and also a memory state map 304. BMM 302 also comprises an interrupt handler in a preferred embodiment, and device 106 interrupts BMM 302

when a packet is received. When a packet is received, using DMA 202 and state map 304, the BMM performs the following tasks:

1. Decides whether a data structure fits into the memory. Whether the structure fits into memory, then, is a function of the size of the data packet and the present state of map 304, which indicates those regions of memory 102 that are available for new data to be stored.
2. If the incoming packet in step 1 above fits into memory, the BMM determines an optimal storage position. It was described above that there are advantages in sequential storage. Because of this, the BMM in a preferred embodiment stores packets into memory 102 in a manner to create a small number of large available regions, rather than a larger number of smaller available regions.
3. BMM 302 notifies processor 100 on path 310 when enough of the packet is stored, so that the processor can begin to perform the desired processing. An identifier for this structure is created and provided to the processor. The identifier communicates at a minimum the starting address of the packet in memory, and in some cases includes additional information.
4. BMM updates map 304 for all changes in the topology of the memory. This updating can be done in any of several ways, such as periodically, or every time a unit in memory is changed.
5. When processing is complete on a packet the BMM has stored in memory 102, the processor notifies BMM 302, which then transfers the processed data back to device 106. This is for the particular example of a

packet processing task. In some other embodiments data may be read out of memory 102 by MM 302 and sent to different devices, or even discarded. In notifying the BMM of processed data, the processor used the data structure identifier previously sent by the BMM upon storage of the data in memory 102.

6. The BMM updates map 304 again, and every time it causes a change in the state of memory 102. Specifically the BMM de-allocates the region or regions of memory previously allocated to the data structure and sets them as available for storage of other data structures, in this case packets.

It will be apparent to the skilled artisan that there may be many alterations in the embodiments described above without departing from the spirit and scope of the present invention. For example, a specific case of operations in a data packet router was illustrated. This is a single instance of a system wherein the invention may provide significant advantages. There are many other systems and processes that will benefit as well. Further, there are a number of ways BMM 302 may be implemented to perform the functionality described above, and there are many systems incorporating many different kinds of processors that might benefit. The present inventors are particularly interested in a system wherein a dynamic multi-streaming processor performs the functions of processor 100. For these reasons the invention should be limited only by the scope of the claims as listed below.

What is claimed is:

1. A background memory manager (BMM) for managing a memory in a data processing system, the BMM comprising:

5 circuitry for transferring data to and from an outside device and to and from a memory;

 a memory state map associated with the memory; and

 a communication link to a processor;

 characterized in that the BMM manages the memory, determining if
10 each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

15 2. The BMM of claim 1 wherein the BMM, in the process of storing each data structure, provides a data identifier for the structure on the link to the processor.

20 3. The BMM of claim 2 wherein the BMM, in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

25 4. The BMM of claim 2 wherein the BMM, in response to a signal on the processor link that the processor is finished with certain identified data in the memory, copies the data from the memory, if needed, to another device, and updates the memory state map to indicate the region of the data copied.

5. The BMM of claim 1 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

5 6. The BMM of claim 1 wherein the data handled by the BMM constitutes network data packets.

7. A data processing system, comprising:

a processor;

10 a memory coupled to the processor; and

a background memory manager coupled to the memory and the processor, the background memory manager including circuitry for transferring data to and from an outside device and to and from the memory, and a memory state map associated with the memory;

15 characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the
20 processor of new data and its location.

8. The data processing system of claim 7 wherein the BMM, in the process of storing data structures in the memory, provides a data identifier for the
25 structure to the processor.

9. The data processing system of claim 8 wherein the BMM, in making memory transactions, updates the memory state map to the new memory

state, keeping track of regions occupied by valid data and regions not occupied by valid data.

5 10. The data processing system of claim 8 wherein the BMM, in response to a signal from the processor that the processor is finished with certain identified data in the memory, copies the data, if necessary, from the memory to another device, and updates the memory state map to indicate the region of the data copied.

10 11. The data processing system of claim 7 further comprising an interrupt handler allowing a remote data source to interrupt the BMM when data is available to be transferred to the memory.

15 12. The data processing system of claim 7 wherein the data handled by the BMM constitutes network data packets.

13. A network packet router, comprising:

an input/output (I/O) device for receiving and sending packets on the network;

20 a processor;

a memory coupled to the processor; and

a background memory manager coupled to the memory and the processor, the background memory manager including circuitry for transferring packets to and from the I/O device and to and from the memory, and a memory state map associated with the memory;

25 characterized in that the BMM manages the memory, determining if each data structure fits into the memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside

device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location.

5 14. The data router of claim 13 wherein the BMM, in the process of storing a packet into the memory, provides a data identifier for the packet to the processor.

10 15. The data router of claim 14 wherein the BMM, in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid packets and regions not occupied by valid packets.

15 16. The data router of claim 14 wherein the BMM, in response to a signal that the processor is finished with a packet in the memory, copies the packet, if necessary, from the memory to the I/O device, and updates the memory state map to indicate the region of the packet copied.

20 17. The data router of claim 13 further comprising an interrupt handler allowing the I/O device to interrupt the BMM when packets are available to be transferred to the memory.

18. A method for managing a memory in a data processing system having a processor, comprising the steps of:

25 (a) transferring data structures to and from an outside device and to and from the memory by circuitry in a background memory manager (BMM);

(b) determining by the BMM if each data structure from the outside device will fit into available space in the memory;

(c) deciding by the BMM exactly where in the memory to store each data structure; and

5 (d) updating a memory state map associated with the memory in the BMM each time a memory transaction is made.

10 19. The method of claim 18 wherein, in step (c), the BMM, in the process of storing a data structure into the memory, provides a data identifier for the structure on the link to the processor.

15 20. The method of claim 19 wherein the BMM, in step (b), in making memory transactions, updates the memory state map to the new memory state, keeping track of regions occupied by valid data and regions not occupied by valid data.

20 21. The method of claim 19 wherein, in step (a), the BMM, in response to a signal that the processor is finished with certain identified data in the memory, copies the data, if necessary, from the memory to another device, and updates the memory state map to indicate the region of the data copied.

25 22. The method of claim 18 further comprising a step for interrupting the BMM by the outside device when data is available to be transferred to the memory.

23. The method of claim 18 wherein the data handled by the BMM constitutes network data packets.

1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2159 2160 2161 2162 2163 2164 2165 2166 2167 2168 2169 2170 2171 2172 2173 2174 2175 2176 2177 2178 2179 2180 2181 2182 2183 2184 2185 2186 2187 2188 2189 2190 2191 2192 2193 2194 2195 2196 2197 2198 2199 2200 2201 2202 2203 2204 2205 2206 2207 2208 2209 2210 2211 2212 2213 2214 2215 2216 2217 2218 2219 2220 2221 2222 2223 2224 2225 2226 2227 2228 2229 2230 2231 2232 2233 2234 2235 2236 2237 2238 2239 2240 2241 2242 2243 2244 2245 2246 2247 2248 2249 2250 2251 2252 2253 2254 2255 2256 2257 2258 2259 2260 2261 2262 2263 2264 2265 2266 2267 2268 2269 2270 2271 2272 2273 2274 2275 2276 2277 2278 2279 2280 2281 2282 2283 2284 2285 2286 2287 2288 2289 2290 2291 2292 2293 2294 2295 2296 2297 2298 2299 2300 2301 2302 2303 2304 2305 2306 2307 2308 2309 2310 2311 2312 2313 2314 2315 2316 2317 2318 2319 2320 2321 2322 2323 2324 2325 2326 2327 2328 2329 2330 2331 2332 2333 2334 2335 2336 2337 2338 2339 2340 2341 2342 2343 2344 2345 2346 2347 2348 2349 2350 2351 2352 2353 2354 2355 2356 2357 2358 2359 2360 2361 2362 2363 2364 2365 2366 2367 2368 2369 2370 2371 2372 2373 2374 2375 2376 2377 2378 2379 2380 2381 2382 2383 2384 2385 2386 2387 2388 2389 2390 2391 2392 2393 2394 2395 2396 2397 2398 2399 2400 2401 2402 2403 2404 2405 2406 2407 2408 2409 2410 2411 2412 2413 2414 2415 2416 2417 2418 2419 2420 2421 2422 2423 2424 2425 2426 2427 2428 2429 2430 2431 2432 2433 2434 2435 2436 2437 2438 2439 2440 2441 2442 2443 2444 2445 2446 2447 2448 2449 2450 2451 2452 2453 2454 2455 2456 2457 2458 2459 2460 2461 2462 2463 2464 2465 2466 2467 2468 2469 2470 2471 2472 2473 2474 2475 2476 2477 2478 2479 2480 2481 2482 2483 2484 2485 2486 2487 2488 2489 2490 2491 2492 2493 2494 2495 2496 2497 2498 2499 2500 2501 2502 2503 2504 2505 2506 2507 2508 2509 2510 2511 2512 2513 2514 2515 2516 2517 2518 2519 2520 2521 2522 2523 2524 2525 2526 2527 2528 2529 2530 2531 2532 2533 2534 2535 2536 2537 2538 2539 2540 2541 2542 2543 2544 2545 2546 2547 2548 2549 2550 2551 2552 2553 2554 2555 2556 2557 2558 2559 2560 2561 2562 2563 2564 2565 2566 2567 2568 2569 2570 2571 2572 2573 2574 2575 2576 2577 2578 2579 2580 2581 2582 2583 2584 2585 2586 2587 2588 2589 2590 2591 2592 2593 2594 2595 2596 2597 2598 2599 2600 2601 2602 2603 2604 2605 2606 2607 2608 2609 2610 2611 2612 2613 2614 2615 2616 2617 2618 2619 2620 2621 2622 2623 2624 2625 2626 2627 2628 2629 2630 2631 2632 2633 2634 2635 2636 2637 2638 2639 2640 2641 2642 2643 2644 2645 2646 2647 2648 2649 2650 2651 2652 2653 2654 2655 2656 2657 2658 2659 2660 2661 2662 2663 2664 2665 2666 2667 2668 2669 2670 2671 2672 2673 2674 2675 2676 2677 2678 2679 2680 2681 2682 2683 2684 2685 2686 2687 2688 2689 2690 2691 2692 2693 2694 2695 2696 2697 2698 2699 2700 2701 2702 2703 2704 2705 2706 2707 2708 2709 2710 2711 2712 2713 2714 2715 2716 2717 2718 2719 2720 2721 2722 2723 2724 2725 2726 2727 2728 2729 2730 2731 2732 2733 2734 2735 2736 2737 2738 2739 2740 2741 2742 2743 2744 2745 2746 2747 2748 2749 2750 2751 2752 2753 2754 2755 2756 2757 2758 2759 2760 2761 2762 2763 2764 2765 2766 2767 2768 2769 2770 2771 2772 2773 2774 2775 2776 2777 2778 2779 2780 2781 2782 2783 2784 2785 2786 2787 2788 2789 2790 2791 2792 2793 2794 2795 2796 2797 2798 2799 2800 2801 2

Abstract of the Disclosure

5 A background memory manager (BMM) for managing a memory in a data processing system has circuitry for transferring data to and from an outside device and to and from a memory, a memory state map associated with the memory, and a communication link to a processor. The BMM manages the memory, determining if each data structure fits into the

10 memory, deciding exactly where to place the data structure in memory, performing all data transfers between the outside device and the memory, and maintaining the memory state map according to memory transactions made, and informing the processor of new data and its location. In preferred embodiments the BMM, in the process of storing data structures

15 into the memory, provides an identifier for each structure to the processor. The system is particularly applicable to Internet packet processing in packet routers.

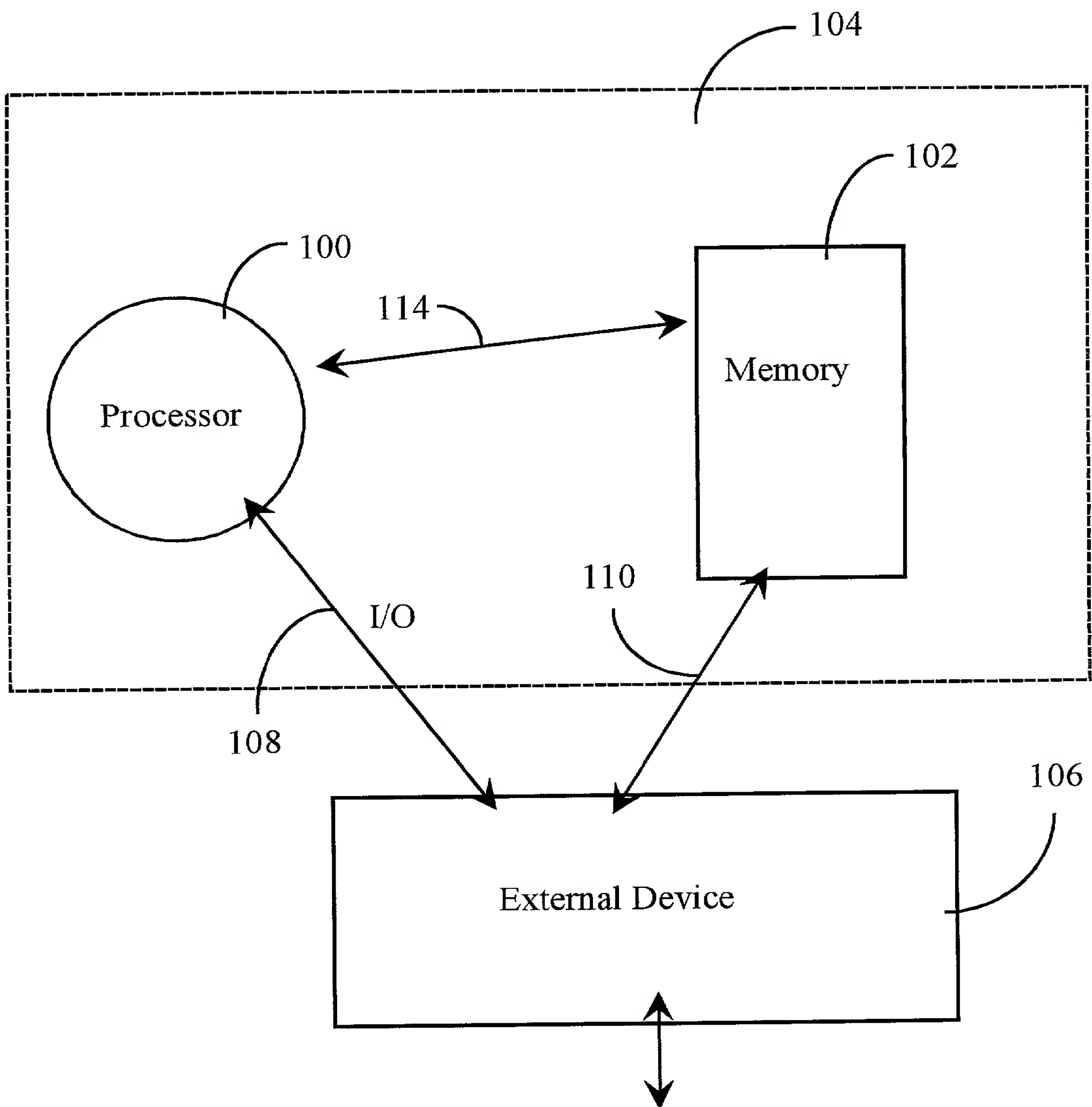


Fig. 1 (Prior Art)

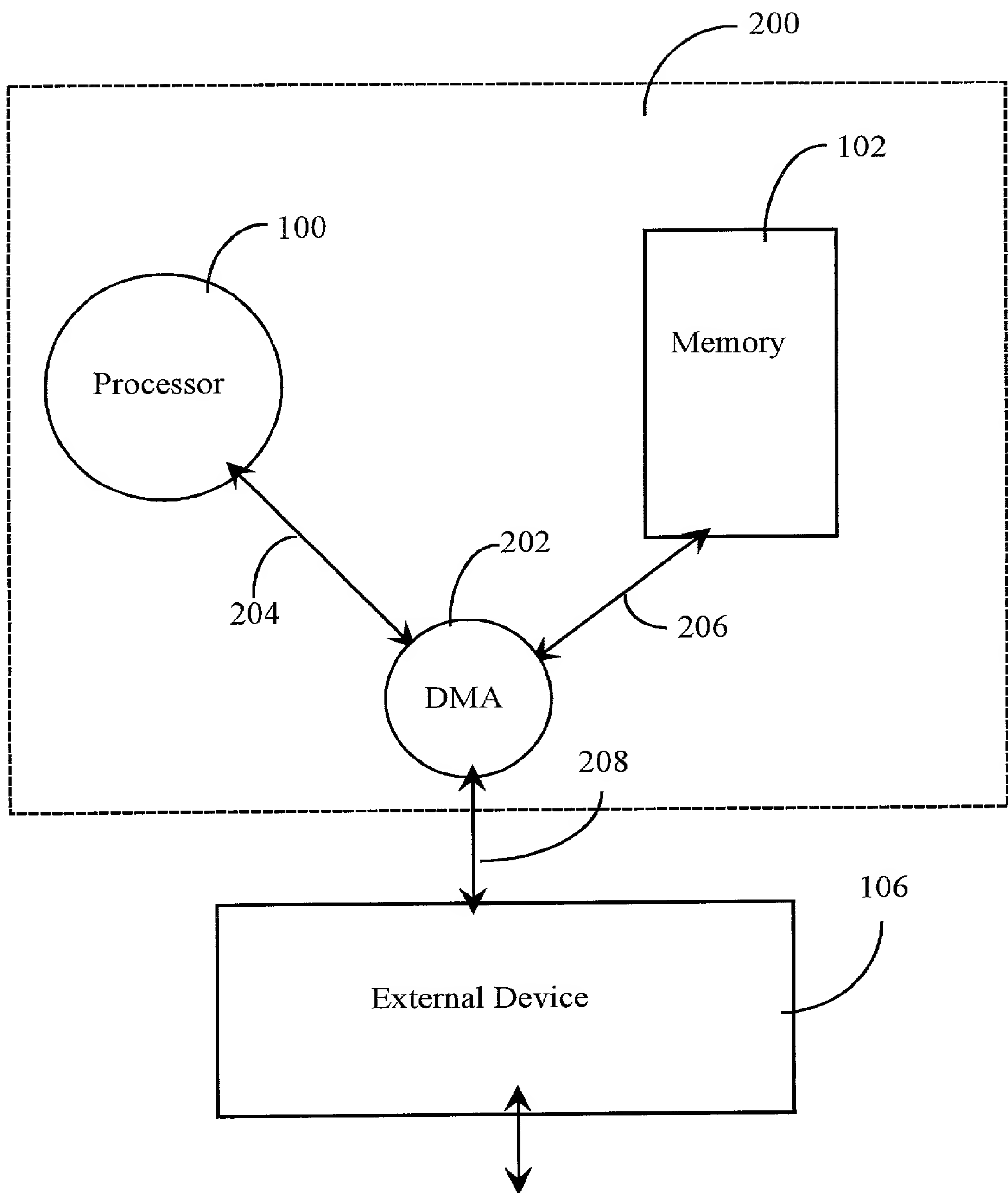


Fig. 2 (Prior Art)

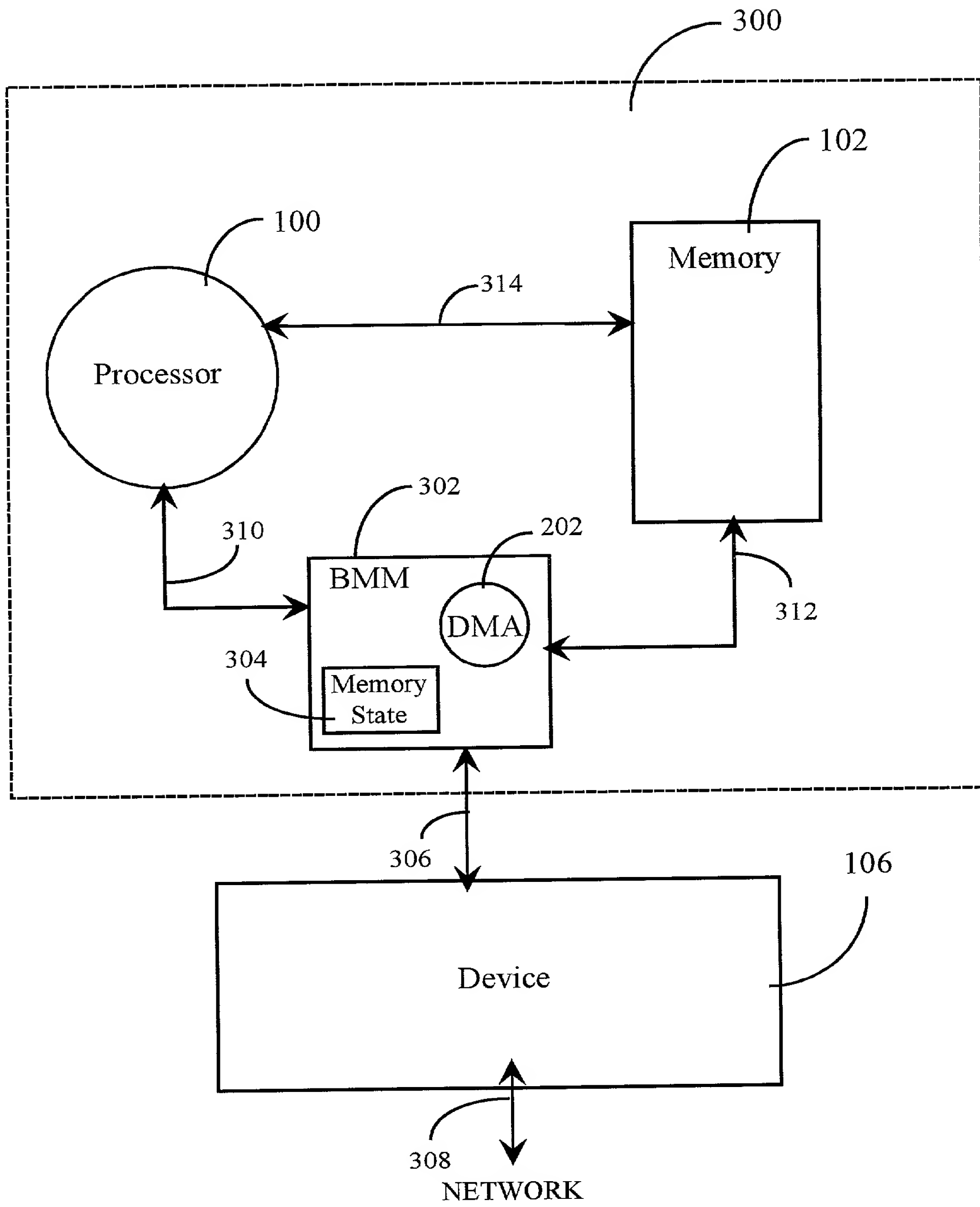


Fig. 3

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO. 3814

As a below named inventor, I hereby declare that: My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods and Apparatus for Background Memory Management

the specification of which (check one) ☒ is attached hereto.
☐ was filed on:
☐ Application Serial No.
☐ and was amended on
(If applicable)

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, s 1.56 (a). In the case that the present application is a continuation-in-part application, I further acknowledge the duty to disclose material information as defined in 37 CFR s 1.56(a) which became available between the filing date of the prior application and the filing date of the present application. I hereby claim foreign priority benefits under Title 35, United States Code s119 of any foreign applications for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)	(Number)	(Country)	(Day/Month/Year Filed)
	(Number)	(Country)	(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, s120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, s112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, s156(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.):	_____	(Filing Date):	_____	(Status):	_____
(Application Serial No.):	_____	(Filing Date):	_____	(Status):	_____
(Application Serial No.):	_____	(Filing Date):	_____	(Status):	_____
(Application Serial No.):	_____	(Filing Date):	_____	(Status):	_____
(Application Serial No.):	_____	(Filing Date):	_____	(Status):	_____

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.
(List name and registration number)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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5th inventor's signature: _____ Dated: _____
Residence: _____ Citizenship: _____
Post Office Address: _____

Full name of 6th joint inventor, if any:

6th inventor's signature: _____ Dated: _____
Residence: _____ Citizenship: _____
Post Office Address: _____

Full name of 7th joint inventor, if any:

7th inventor's signature: _____ Dated: _____
Residence: _____ Citizenship: _____
Post Office Address: _____

Full name of 8th joint inventor, if any:

8th inventor's signature: _____ Dated: _____
Residence: _____ Citizenship: _____
Post Office Address: _____